Amendments to the Claims

1. (*Original*) Apparatus (20; 30; 41) for performing a temperature measurement function, comprising a first stage with

a first circuit (11) and a second circuit (12) being arranged in parallel,

said first circuit (11) comprising a first transistor (Ml) , a first resistor (R_{temp}) , and a parallel arrangement of n diodes (B1 - Bn),

said second circuit (12) comprising a second transistor (M2) and a parallel arrangement of m diodes (C2),

an operational amplifier (13) on the input side being connected to the first circuit (11) and the second circuit (12), said operational amplifier (13) applying a gate voltage to said first transistor (Ml) and said second transistor (M2),

said apparatus (20; 30; 41) further comprising an output stage with p output transistors (N1 - Np), and an output resistor ($r*R_{temp}$) performing a current to output voltage conversion in order to provide an output voltage ($V_{tempout}$) that depends on the actual temperature (T).

2. (*Original*) The Apparatus (20; 30; 41) of claim 1, wherein said first transistor (Mi) provides a first current (Il) flowing through the parallel arrangement of n diodes (Bi - Bn) and said second transistor (M2) provides a second current (12) flowing through the parallel arrangement of m diodes (C2).

3. (*Previously Presented*) The Apparatus (20; 30; 41) of claim 1 , wherein said operational amplifier (13) has a first input (15), a second input (14), and an output (16), the first input (15) being connected to a drain of the first transistor (M1) and the second input (14) being connected to a drain of the second transistor (M2), said output (16) being connected to a gate of said first transistor (Ml) and a gate of said second transistor (M2) for biasing these transistors (M1, M2).

4. (*Previously Presented*) The Apparatus (20; 30; 41) of claim 1, wherein said output stage amplifies ~~said first~~ a first current (I1) to obtain a third current (13) before

performing said current to output voltage conversion by converting said third current (13) into said output voltage ($V_{tempout}$)

5. (*Previously Presented*) The Apparatus (20; 30; 41) of claim 1 wherein said first resistor (R_{temp}) and said output resistor ($r*R_{temp}$) are both either integrated Npoly resistors or integrated Ppoly resistors.

6. (*Previously Presented*) The Apparatus (20; 30; 41) of claim 1, wherein said output resistor (R_{temp}) is realized by a plurality of r resistors, the resistance of the output resistor ($r*R_{temp}$) being r times the resistance of said first resistor (R_{temp}), r being an integer number.

7. (*Previously Presented*) The Apparatus (20; 30; 41) of claim 1, comprising a hold-capacitor (C) being arranged in parallel to the output resistor ($r*R_{temp}$) in order to filter out noise and/or to stabilize said output voltage ($V_{tempout}$)

8. (*Previously Presented*) The Apparatus (20; 30; 41) of claim 1, wherein said first transistor (M1) and said output transistors (N1 – Np), as well as said first resistor (R_{temp}) and output resistor ($r*R_{temp}$) are designed to minimize mismatch effects.

9. (*Previously Presented*) The Apparatus (20; 30; 41) of claim 1, wherein said number n, m and p are integer numbers.

10. (*Previously Presented*) The Apparatus (20; 30; 41) of claim 1, wherein diode-connected PNP bipolar transistors (B1 – Bn, C2) serve as diodes.

11. (*Previously Presented*) The Apparatus (20; 30; 41) of claim 1, wherein said operational amplifier (13) is a low-offset operational amplifier.

12. (*Previously Presented*) The Apparatus (20; 30; 41) of claim 1, wherein the output voltage Vtempout) and the actual temperature (T) have a linear dependency.

13. (*Previously Presented*) The Apparatus (20; 30; 41) of claim 1, wherein the gate voltage is applied to gates of the p output transistors (Ni - Np).

14. (*Previously Presented*) The Apparatus (30) of claim 1 further comprising a temperature compensation network (31) providing a bandgap reference voltage (V_{bgp}) at another output (36).

15. (*Original*) The Apparatus (30) of claim 14, wherein the temperature compensation network (31) comprises a plurality of voltage followers (32, 33, 34) with an implemented offset, the voltage followers (32, 33, 34) being connected in series.

16. (*Currently Amended*) Device (40) ~~comprising~~ including an apparatus (41) according to claim 1.

17. (*Original*) The device (40) of claim 16, further comprising an analog-to-digital converter (42).

18. (*Currently Amended*) The device (40) of claim 16 being part of a circuit, the circuit including at least one of the following: an analog device, a mixed-mode device, or a digital device.